PMC Precision MicroControl Corp.

TechNOTE

Title: Command Interpreter Status Bits
Products(s): DCX-AT200/300 and DCX-VM200/300
Keywords: DCX-AT200, DCX-AT300, DCX-VM200, DCX-VM300, Status
ID#: TN1036
Date: June 20, 2001

Summary
The command interpreter status bits allow the host computer to monitor certain conditions on the motion controller. The meaning and location of these status bits is described in this tech note and the included tables.

More Information
The command interpreter status bits are located in the dual port memory of the DCX controller. This memory has 4096 bytes that are visible to the host computer. The status bits are located in the bytes at offset 808 hex and 809 hex. The DCX controller User's Manual provides details on where the dual port memory will be located in the host computer's address space.

There are 4 possible command interfaces on a DCX-AT or DCX-VM controller: Host PC Binary, Host PC ASCII, Serial (RS-232), and GPIB (IEEE-488). Each of these command interfaces has corresponding Busy and Error status bits. The Busy bit will be set when the controller receives a command sequence on the respective interface. This bit will be cleared when the controller completes execution of the commands.

IMPORTANT NOTE: When the host computer is sending command strings to the PC ASCII interface of the DCX controller, it is necessary for it to wait for the Busy bit to clear before sending each command string. The other interfaces use different means to hold off commands.

The Error status bit will be set if the controller encounters an error while trying to interpret or execute the commands. To clear an error bit, the Tell Error command must be issued to the same command interface that has the error.

The Host PC ASCII interface and the Serial Interface include Single Stepping status bits. These will be set when the respective interface is put into single stepping mode by sending a space character. It will be cleared when the command interface returns to normal operation.

Certain commands place the respective interface into a file load mode. There is a Loading File status bit for each of the interfaces that support this. The bit will be set when the load command is executed, and stay set until End-Of-Text (ASCII 3) character is received.

The following 2 tables list the command interpreter status bits for the DCX controllers. Note that the bit locations are different for the DCX-AT and DCX-VM controllers. This is a result of the "little endian" versus "big endian" byte ordering on the respective controllers.

DCX-AT200/300 Command Interpreter Status Bits

Offset	Bit	Description
808h	0	Host PC Binary Interface – Busy
808h	1	Host PC Binary Interface – Error
808h	2	Unused
808h	3	Unused
808h	4	Host PC ASCII Interface – Busy
808h	5	Host PC ASCII Interface – Error
808h	6	Host PC ASCII Interface – Single Stepping
808h	7	Host PC ASCII Interface – Loading File
809h	0	Serial (RS-232) Interface – Busy
809h	1	Serial (RS-232) Interface – Error
809h	2	Serial (RS-232) Interface – Single Stepping
809h	3	Serial (RS-232) Interface – Loading File
809h	4	GPIB (IEEE-488) Interface – Busy
809h	5	GPIB (IEEE-488) Interface – Error
809h	6	Unused
809h	7	GPIB (IEEE-488) Interface – Loading File

DCX-VM200/300 Command Interpreter Status Bits

Offset	Bit	Description
808h	0	Serial (RS-232) Interface – Busy
808h	1	Serial (RS-232) Interface – Error
808h	2	Serial (RS-232) Interface – Single Stepping
808h	3	Serial (RS-232) Interface – Loading File
808h	4	GPIB (IEEE-488) Interface – Busy
808h	5	GPIB (IEEE-488) Interface – Error
808h	6	Unused
808h	7	GPIB (IEEE-488) Interface – Loading File
809h	0	Host PC Binary Interface – Busy
809h	1	Host PC Binary Interface – Error
809h	2	Unused
809h	3	Unused
809h	4	Host PC ASCII Interface – Busy
809h	5	Host PC ASCII Interface – Error
809h	6	Host PC ASCII Interface – Single Stepping
809h	7	Host PC ASCII Interface – Loading File